

Inventor: Doi, Yutaka
Serial No.: 09/752,660
Client Ref. No. H0001384 (4970)
Our Ref. No. 100665.0026US1



Art Unit: 2841
Examiner: Patel, Ishwarbhai B.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231**

Inventor: **Doi, Yutaka**
Serial No: **09/752,660**
Filed: **December 28, 2000**
For: **Layered Circuit Boards
and Methods of
Production Thereof**

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RESPONSE TO OFFICE ACTION

The Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

This paper responds to the Office Action dated July 18, 2002. Please enter the following:

IN THE CLAIMS

Amend claim 11 as shown.

- B¹
11. The electronic component of claim 1, further comprising a first embedded passive component in the first etched compartment and a second embedded passive component in the second etched compartment wherein the first passive component is a capacitor comprising the capacitor material and the second passive component is a resistor comprising the resistor material.

IN THE SPECIFICATION

Amend the section "Brief Description of the Drawings" on page 4 by replacing the

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description for figure 4, and adding a description for figure 5 as follows:

B²
--Fig. 4 is a graphical diagram of a preferred method and embodiment.

Fig. 5 is a cutaway view of the graphical diagram of figure 4.--

Replace the paragraph beginning on page 7, line 28 with the following:

B³
--Figure 3 shows a preferred method 200 of preparing the layered component comprising an insulator layer having embedded passive components of two different kinds of materials. A substrate layer 100 is prepared 210 that forms the basis for the component contemplated herein. A metal trace or patterned metal layer 102 is laid down 220 as part of the substrate layer 100. An insulator layer 110 is laminated 230 onto the substrate layer 100. The insulator layer is imaged 240 creating an etching pattern 242 for the resistor 120. The imaged insulator layer 110 is etched 250 to create a compartment 122 for the resistor 120 while exposing a portion of the metal layer 102 that had been previously laid down as part of the substrate layer 100. The compartment 122 is filled 260 with the resistor material or paste 124. The insulator layer 110 is further imaged 270 creating an etching pattern 272 for the capacitor 130. The imaged insulator layer 110 is etched 280 to create a compartment 132 for the capacitor 130 while exposing a portion of the metal layer 102 that had been previously laid down as part of the substrate layer 100. The compartment 132 is filled 290 with the capacitor material or paste 154. Additional layers can then be added 300 to the finished insulator layer 110. A graphical diagram of this preferred method and preferred embodiment of the subject matter described herein is shown by the detailed example in Figures 4 and 5.--

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REMARKS

Specification Amendments

The disclosure was objected to as failing to reference Figure 5. This objection is moot in light of the amendments contained herein adding such references.

35 USC § 112

Claim 11 was rejected as being indefinite. This rejection is moot in light of the amendments to claim 11 contained herein.

35 USC § 102

Claims 1-5, 9, 11, and 12 were rejected under 35 USC § 102(e) as being anticipated by Felton (US 6317023). The applicant disagrees as Felton fails to teach or suggest all of the recitations of claim 11.

As previously pointed out by Applicant, claim 1 (and claims 6-12 by virtue of their dependence on claim 1) all include the recitation of "...the insulator layer comprises ... a first etched compartment filled with a capacitor material, and a second etched compartment filled with a resistor material...." Felton does not teach or suggest a component comprising an *etched compartment* filled with a capacitor material and/or an *etched compartment* filled with a resistor material. As such, at least for these reasons, Felton does not teach or suggest all the recitations of claim 1 and therefore does not anticipate claim 1 or any claim dependent on claim 1.

The Office attempts to rebut Applicant's arguments by pointing out that describing the phrase "etched compartment" is a process limitation in an article claim, and that the patentability of a product does not depend on its method of production. Applicant does not dispute this. However, the Office fails to follow through in its arguments and appears to come to a conclusion that is not supported. The test, as stated by the Office, is that "[i]f the product-by-process claim is the same as or obvious from a product of the prior art, the claim is upatentable even though the prior product was made by a different process. Yet the Office fails to assert, and rightly so, that the claimed product is the same as or obvious from a prior art product. An etched compartment is structurally different from a compartment formed by forcing hardened components into an

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adhesive layer as taught by Felten, thus Felten does not anticipate the claimed component. Moreover, an electronic component having an etched compartment is not obvious in light of an electronic component having compartments formed by forcing hardened components into an adhesive layer. As such, claim 1 is not anticipated by or obvious over the cited references, nor are claims 2-12 at least because of their dependence on claim 1.

35 USC § 103

Claims 6-8 and 10 were rejected under 35 USC § 103 as being obvious over Felton in view of Van De Walle et al. (US5731747, herein referred to as Van De Walle). The applicant disagrees, especially in view of the amendments set forth herein. Among other things, claims 6-8 and 10 are all allowable as being dependent upon allowable claims.

ATTACHED MARKED-UP VERSION OF CHANGES

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".


REQUEST FOR ALLOWANCE

Claims 1-12 are pending in this application. The applicant requests allowance of all pending claims.

Respectfully submitted,

Rutan & Tucker, LLP

Dated: September 26, 2002

By: 
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